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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,128	WILSON ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed July 03, 2003 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings filed July 03, 2003 are accepted.

Specification

The specification filed July 03, 2003 is accepted.

Claim Rejections - 35 USC § 103

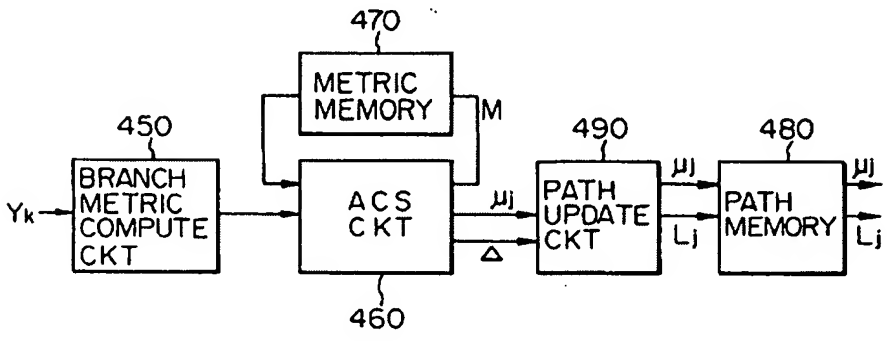
The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katsuragawa et al. (USPN 5907586).

As per claim 1, Katsuragawa et al. (herein after: Katsuragawa) substantially teaches a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal.

Fig. 7



Katsuragawa teaches (Figures 6-7) the decoders 410-41N each has a branch metric compute circuit 450, an ACS circuit 460, a metric memory 470, a path memory 480, and a path update

circuit 490. A received symbol Yk is input to the branch metric compute circuit 450. In response, the compute circuit 450 produces branch metrics on the basis of the symbol Yk and its estimate Xk. The ACS circuit 460 adds up branch metrics sequentially applied thereto from the compute circuit 450, and compares the resulting path metrics so as to sequentially select valid paths. Particularly, in the illustrative embodiment, when the ACS circuit 460 has selected one of a plurality of paths at each branch, it determines a difference between the greatest metric and the smallest metric at the branch and outputs it together with the path selected.

Katsuragawa does not explicitly teach the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions as stated in the present application.

However, Katsuragawa teaches (cols. 12-13) the convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of 2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to **a two-bit one-symbol** convolutional code with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150. Katsuragawa also teaches (col. 8) during the course of trellis tracing, the branch metric computing section determines the metrics of consecutive branches represented by differences

between the values which the coded signal may take and the actual value of the received symbol, e.g., Hamming distances or Euclidean distances. The adding section adds the metrics produced at the preceding branch to the metrics produced at the current branch. The comparing circuit compares the resulting path metrics. The selecting circuit sequentially selects valid paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions within the teachings of Katsuragawa. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by shifting the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions would refresh the ACS circuit in a time-efficient manner.

As per claim 2, Katsuragawa substantially teaches, in view of above rejections, (figure 1) a plurality of add-compare-select circuits that feed instructions into the M break-off circuit 30.

As per claim 3, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path.

As per claims 4 and 5, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The Examiner would like to point out that a comparison has to be done between at least two add operations. The selection process follows the comparison.

As per claim 6, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. Further, in Figure 1 Katsuragawa teaches the add-compare-select operations to be performed in parallel.

As per claim 7, Katsuragawa substantially teaches, in view of above rejections, an M break-off circuit sequentially receives a plurality of path metrics sequentially detected by the plurality of Viterbi decoders during the trellis tracings, and sequentially breaks off the trellis tracings of, among the plurality of paths, unlikely paths to thereby detect M most probable paths over at least two of the plurality of Viterbi decoders. A decision circuit performs the final decision with the path metrics of the M paths to thereby determine which of the decoded signals output from the plurality of Viterbi decoders has a correct code rate.

As per claim 8, Katsuragawa substantially teaches, in view of above rejections, Figure 7, that following each add-compare-select unit is a path update circuit and therefore for each received signal a update is perform.

As per claim 9, Katsuragawa substantially teaches, in view of above rejections, Figure 7, that following each add-compare-select unit is a path update circuit and therefore for each received signal a update is perform.

As per claim 10, Katsuragawa substantially teaches a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are

sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Katsuragawa teaches (Figures 6-7) the decoders 410-41N each has a branch metric compute circuit 450, an ACS circuit 460, a metric memory 470, a path memory 480, and a path update circuit 490. A received symbol Yk is input to the branch metric compute circuit 450. In response, the compute circuit 450 produces branch metrics on the basis of the symbol Yk and its estimate Xk. The ACS circuit 460 adds up branch metrics sequentially applied thereto from the compute circuit 450, and compares the resulting path metrics so as to sequentially select valid paths. Particularly, in the illustrative embodiment, when the ACS circuit 460 has selected one of a plurality of paths at each branch, it determines a difference between the greatest metric and the smallest metric at the branch and outputs it together with the path selected.

Katsuragawa does not explicitly teach the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions as stated in the present application.

However, Katsuragawa teaches (cols. 12-13) the convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of

2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to **a two-bit one-symbol** convolutional code with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150. Katsuragawa also teaches (col. 8) during the course of trellis tracing, the branch metric computing section determines the metrics of consecutive branches represented by differences between the values which the coded signal may take and the actual value of the received symbol, e.g., Hamming distances or Euclidean distances. The adding section adds the metrics produced at the preceding branch to the metrics produced at the current branch. The comparing circuit compares the resulting path metrics. The selecting circuit sequentially selects valid paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions within the teachings of Katsuragawa. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by shifting the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions would refresh the ACS circuit in a time-efficient manner.

As per claim 11, Katsuragawa substantially teaches, in view of above rejections, (figure 1) a plurality of add-compare-select circuits that feed instructions into the M break-off circuit 30.

As per claim 12, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path.

As per claims 13 and 14, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The Examiner would like to point out that a comparison has to be done between at least two add operations. The selection process follows the comparison.

As per claim 15, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. Further, in Figure 1 Katsuragawa teaches the add-compare-select operations to be performed in parallel.

As per claim 16, Katsuragawa substantially teaches, in view of above rejections, an M break-off circuit sequentially receives a plurality of path metrics sequentially detected by the plurality of Viterbi decoders during the trellis tracings, and sequentially breaks off the trellis tracings of, among the plurality of paths, unlikely paths to thereby detect M most probable paths over at least two of the plurality of Viterbi decoders. A decision circuit performs the final decision with the path metrics of the M paths to thereby determine which of the decoded signals output from the plurality of Viterbi decoders has a correct code rate.

As per claim 17, Katsuragawa substantially teaches a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Katsuragawa teaches (Figures 6-7) the decoders 410-41N each has a branch metric compute circuit 450, an ACS circuit 460, a metric memory 470, a path memory 480, and a path update circuit 490. A received symbol Yk is input to the branch metric compute circuit 450. In response, the compute circuit 450 produces branch metrics on the basis of the symbol Yk and its estimate Xk. The ACS circuit 460 adds up branch metrics sequentially applied thereto from the compute circuit 450, and compares the resulting path metrics so as to sequentially select valid paths. Particularly, in the illustrative embodiment, when the ACS circuit 460 has selected one of a plurality of paths at each branch, it determines a difference between the greatest metric and the smallest metric at the branch and outputs it together with the path selected.

Katsuragawa does not explicitly teach the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions as stated in the present application.

However, Katsuragawa teaches (cols. 12-13) the convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of 2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to **a two-bit one-symbol** convolutional code with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150. Katsuragawa also teaches (col. 8) during the course of trellis tracing, the branch metric computing section determines the metrics of consecutive branches represented by differences between the values which the coded signal may take and the actual value of the received symbol, e.g., Hamming distances or Euclidean distances. The adding section adds the metrics produced at the preceding branch to the metrics produced at the current branch. The comparing circuit compares the resulting path metrics. The selecting circuit sequentially selects valid paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions within the teachings of Katsuragawa. This modification would have been obvious to

one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by shifting the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions would refresh the ACS circuit in a time-efficient manner.

As per claim 18, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. Further, in Figure 1 Katsuragawa teaches the add-compare-select operations to be performed in parallel.

As per claim 19, Katsuragawa substantially teaches, in view of above rejections, a plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. Further, in Figure 1 Katsuragawa teaches the add-compare-select operations to be performed in parallel.

As per claim 20, Katsuragawa substantially teaches, in view of above rejections, a signal decision device for a coding communication system and for identifying the code rate of a received signal encoded at any one of a plurality of code rates including a convolutional code rate has a plurality of soft output Viterbi decoders for respectively performing trellis tracings with the received signal in accordance with the plurality of code rate to thereby decode the received signal to a plurality of signals each having a particular rate, and outputs together with the plurality of signals reliability information representative of the likelihood of the plurality of signals. A decision circuit determines, based on the reliability information received from the plurality of soft output Viterbi decoders, which of the plurality of signals is correct.

As per claim 21, Katsuragawa substantially teaches a method and a device for signal decision, a receiver and a channel condition estimating method for a coding communication system are disclosed. A plurality of add, compare and select (ACS) circuits each sequentially determines metrics at a particular trellis tracing rate assigned thereto. The metrics are sequentially added in order to select the most probable path. An M break-up circuit 30 compares the path metrics of the most probable paths and breaks up unlikely paths over a plurality of circuits. The path metrics of probable paths are sequentially written to respective metric memories and again fed to the ACS circuits for trellis tracings. This is repeated until the M break-up circuit 30 selects M paths out of paths fed from N (N>M) ACS circuits. The M paths are delivered to a decision circuit while survivor paths are written to respective path memories. The decision circuit selects one of the M path metrics having the smallest value, reads the path out of the path memory, traces it back, and then outputs decoded bits via an output terminal. Katsuragawa teaches (Figures 6-7) the decoders 410-41N each has a branch metric compute circuit 450, an ACS circuit 460, a metric memory 470, a path memory 480, and a path update circuit 490. A received symbol Yk is input to the branch metric compute circuit 450. In response, the compute circuit 450 produces branch metrics on the basis of the symbol Yk and its estimate Xk. The ACS circuit 460 adds up branch metrics sequentially applied thereto from the compute circuit 450, and compares the resulting path metrics so as to sequentially select valid paths. Particularly, in the illustrative embodiment, when the ACS circuit 460 has selected one of a plurality of paths at each branch, it determines a difference between the greatest metric and the smallest metric at the branch and outputs it together with the path selected.

Katsuragawa does not explicitly teach the update logic is configured to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions as stated in the present application.

However, Katsuragawa teaches (cols. 12-13) the convolutional encoder 130 transforms the 1.2 kbps, 2.4 kbps, 4.8 kbps and 9.6 kbps speech codes to convolutional codes having rates of 2.4 kilosymbols per second (ksps), 4.8 ksps, 9.6 ksps and 19.2 ksps, respectively. In this specific arrangement, the convolutional encoder 130 is a rate 1/2 encoder for transforming each bit of the speech code to **a two-bit one-symbol** convolutional code with a preselected algorithm. A repeat circuit 140 repeats the 2.4 ksps signal eight consecutive times. The repeat circuit 140 repeats the 4.8 ksps signal four consecutive times. Further, the repeat circuit 140 repeats the 9.6 ksps signal twice. As a result, all the signals of 2.4 ksps to 19.2 ksps are output from the repeat circuit 140 with the common rate of 19.2 ksps. In this sense, the repeat circuit 140 plays the role of a rate converting circuit. The 19.2 ksps signals are fed to an interleaver or signal convert circuit 150. Katsuragawa also teaches (col. 8) during the course of trellis tracing, the branch metric computing section determines the metrics of consecutive branches represented by differences between the values which the coded signal may take and the actual value of the received symbol, e.g., Hamming distances or Euclidean distances. The adding section adds the metrics produced at the preceding branch to the metrics produced at the current branch. The comparing circuit compares the resulting path metrics. The selecting circuit sequentially selects valid paths. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to shift the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions within the teachings of Katsuragawa. This modification would have been obvious to

one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by shifting the contents of the register 2 bit positions in order to vacate 2 consecutive bit positions would refresh the ACS circuit in a time-efficient manner.

As per claim 22, Katsuragawa substantially teaches, in view of above rejections, a signal decision device for a coding communication system and for identifying the code rate of a received signal encoded at any one of a plurality of code rates including a convolutional code rate has a plurality of soft output Viterbi decoders for respectively performing trellis tracings with the received signal in accordance with the plurality of code rate to thereby decode the received signal to a plurality of signals each having a particular rate, and outputs together with the plurality of signals reliability information representative of the likelihood of the plurality of signals. A decision circuit determines, based on the reliability information received from the plurality of soft output Viterbi decoders, which of the plurality of signals is correct.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
October 20, 2005

GUY LAMARRE
PRIMARY EXAMINER